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(54) PACKAGING FOR AN ELECTRONIC DEVICE

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CPC ***H01L 43/04*** (2013.01); ***G01R 15/207*** (2013.01); ***G01R 33/0052*** (2013.01); ***G01R 33/09*** (2013.01); ***H01L 21/4828*** (2013.01); *G01R 15/202* (2013.01); *H01L 23/49548* (2013.01); *H01L 24/13* (2013.01); *H01L 24/16* (2013.01); *H01L 24/81* (2013.01); *H01L 43/065* (2013.01); *H01L 2224/131* (2013.01); *H01L 2224/16245* (2013.01); *H01L 2224/81801* (2013.01); *H01L 2924/15162* (2013.01)

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CPC H01L 43/04; H01L 43/06; H01L 43/065; G01R 33/0047

USPC .... 324/117 H, 251; 257/427

See application file for complete search history.

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Assistant Examiner — Scott Stowe
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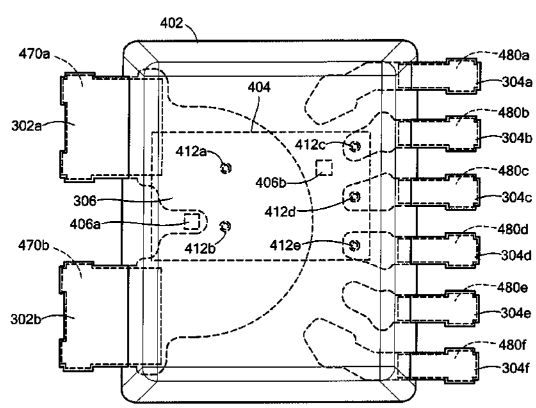
(57) **ABSTRACT**

In one aspect, a method includes processing a metal substrate, performing a first etch on a first surface of the metal substrate to form, for an integrated circuit package, secondary leads and a curved component having two primary leads and performing a second etch, on a second surface of the substrate opposite the first surface, at locations on the secondary leads and locations on the curved component to provide a locking mechanism. Each primary lead located at a respective end of the curved component.

12 Claims, 7 Drawing Sheets



(51) **Int. Cl.**

G01R 33/00	(2006.01)
G01R 33/09	(2006.01)
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H01L 23/495	(2006.01)
H01L 23/00	(2006.01)

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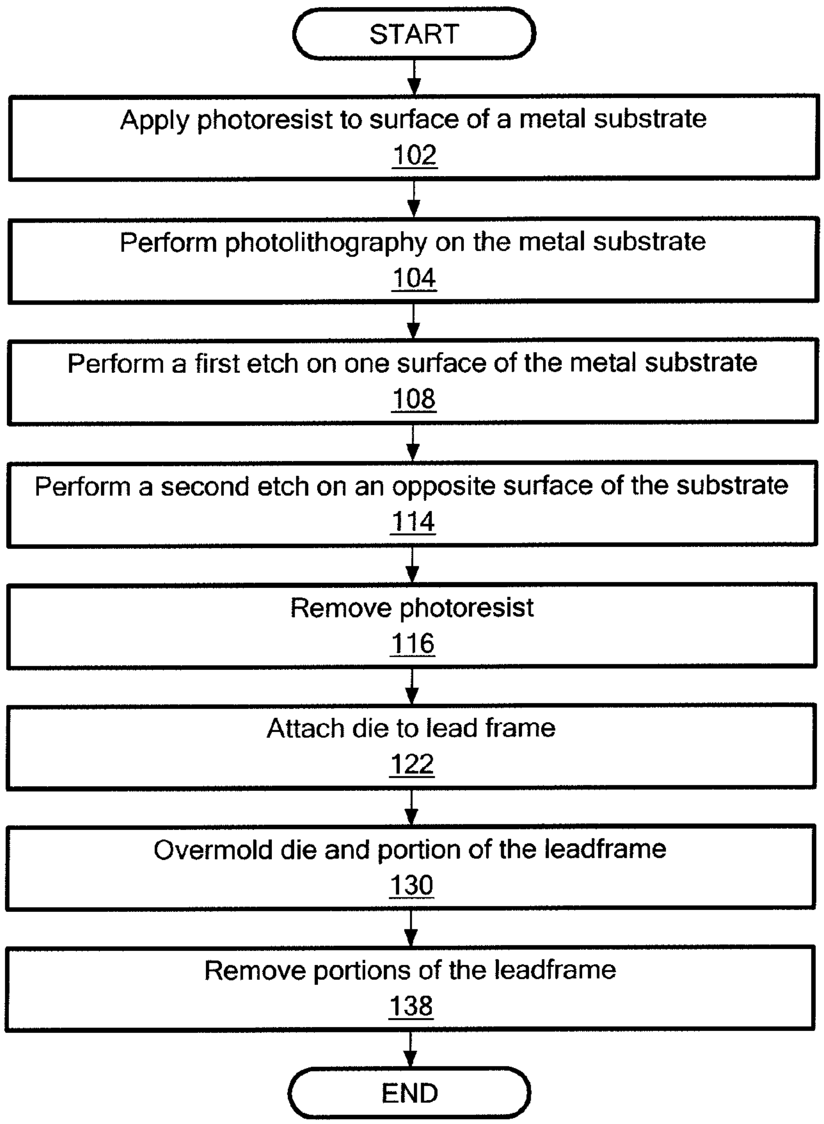
START
Apply photoresist to surface of a metal substrate
102
Perform photolithography on the metal substrate
104
Perform a first etch on one surface of the metal substrate
108
Perform a second etch on an opposite surface of the substrate
114
Remove photoresist
116
Attach die to lead frame
122
Overmold die and portion of the leadframe
130
Remove portions of the leadframe
138
END

FIG. 1

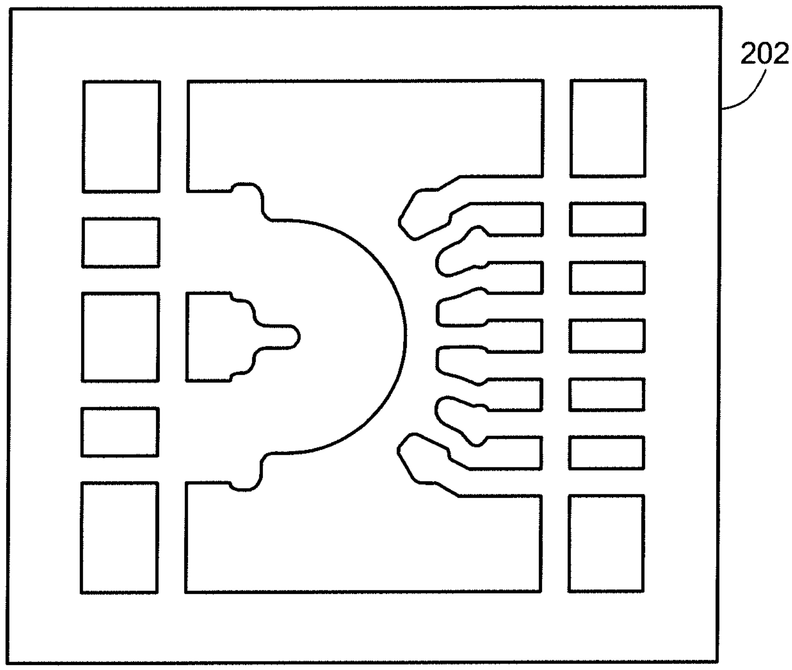

FIG. 2A

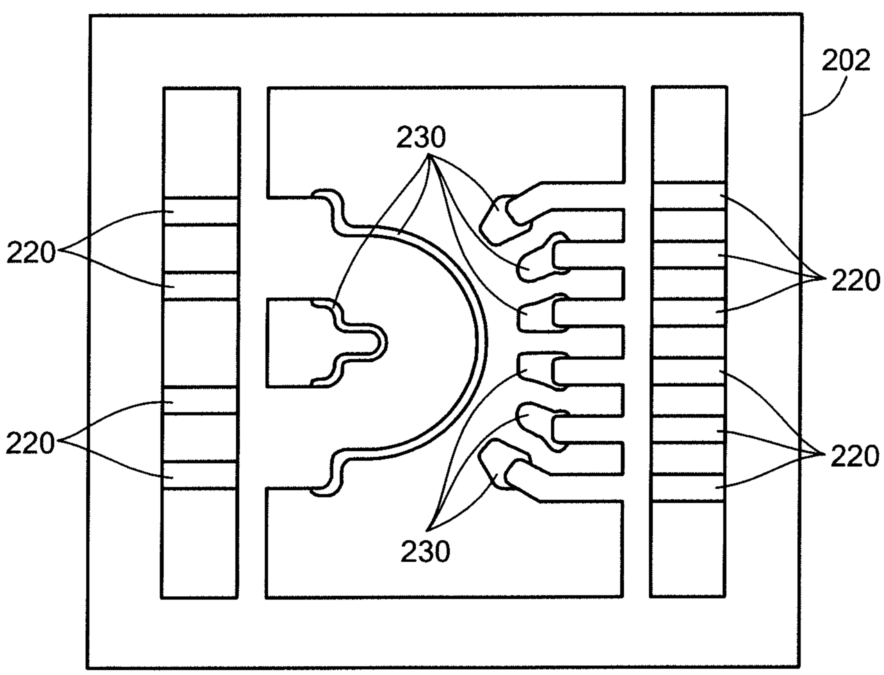

FIG. 2B

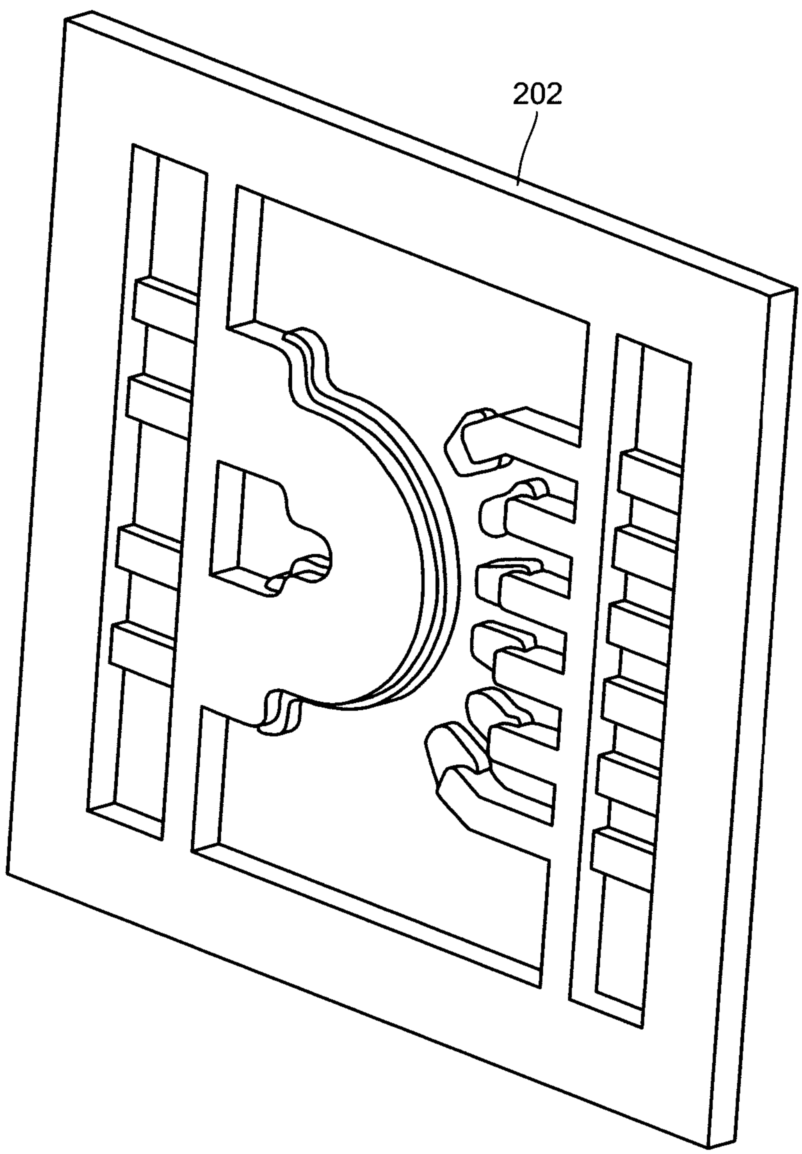

FIG. 2C

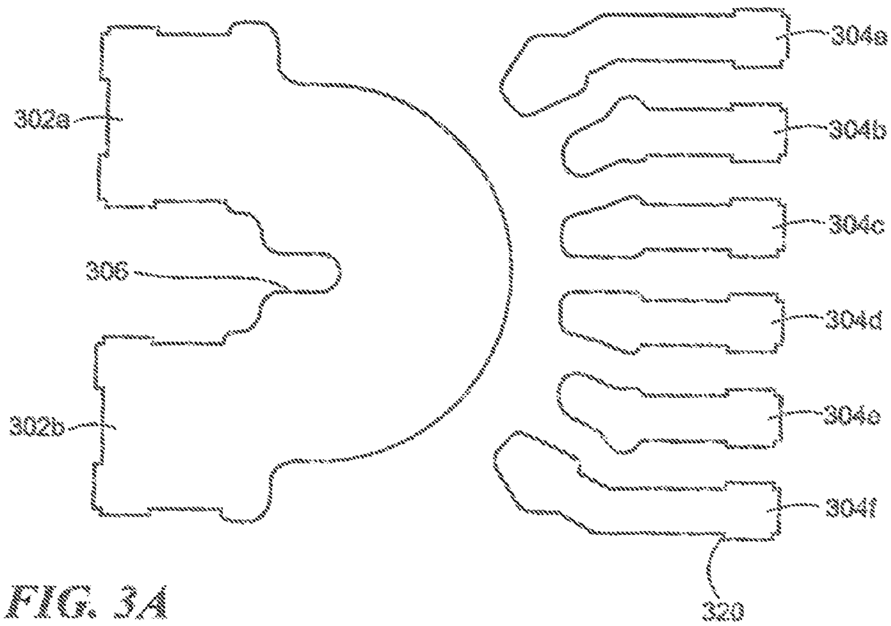
304a
304b
302a
304c
306
304d
302b
304e
304f
320

FIG. 3A

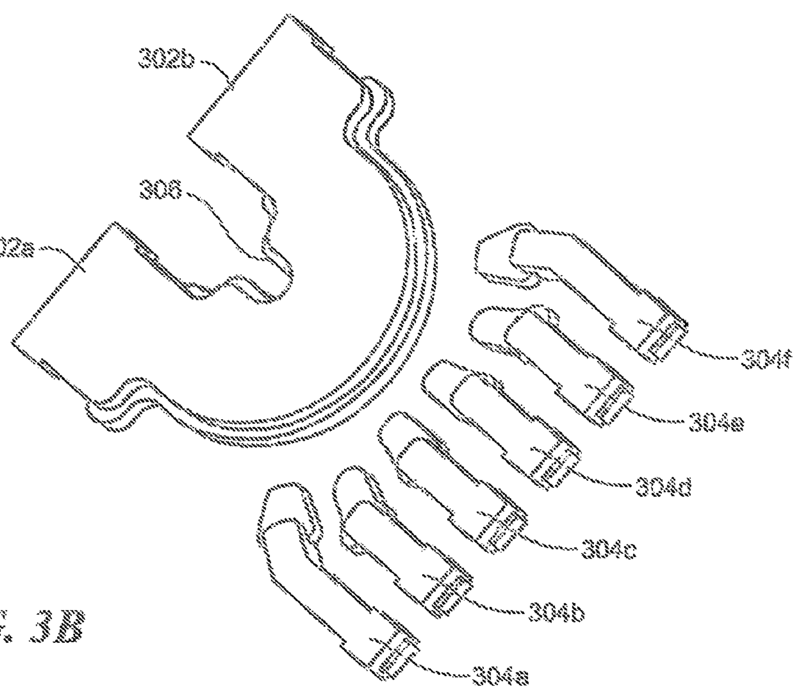
302b
306
302a
304f
304e
304d
304c
304b
304a

FIG. 3B

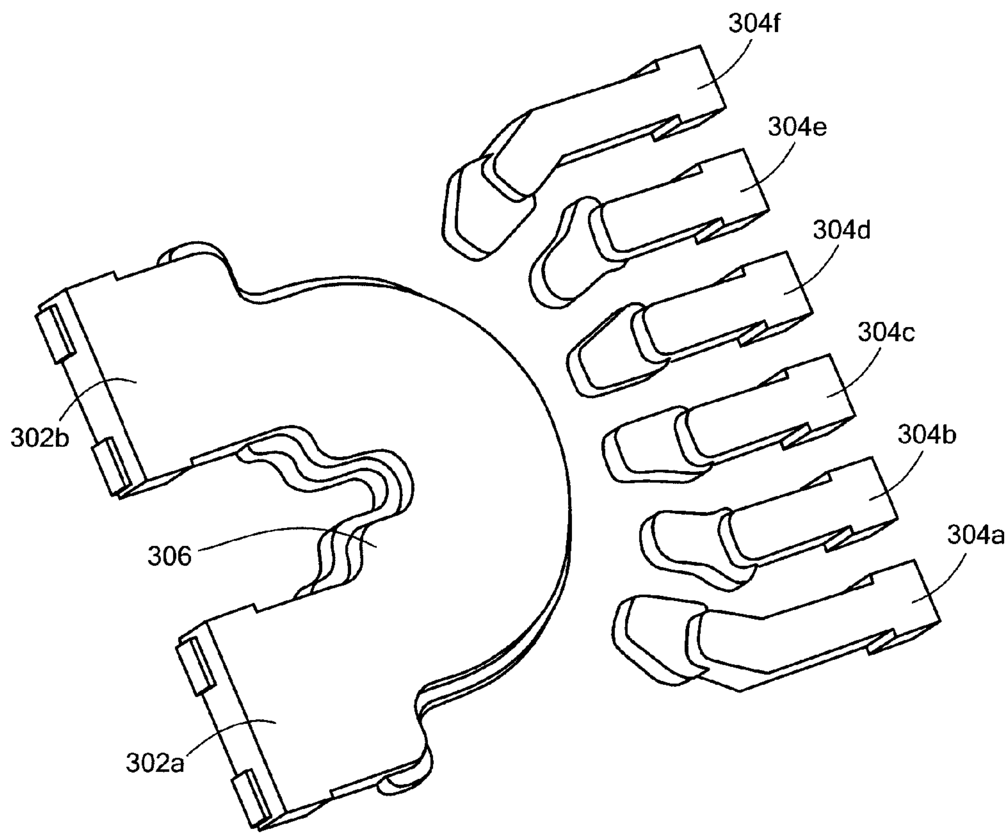

FIG. 3C

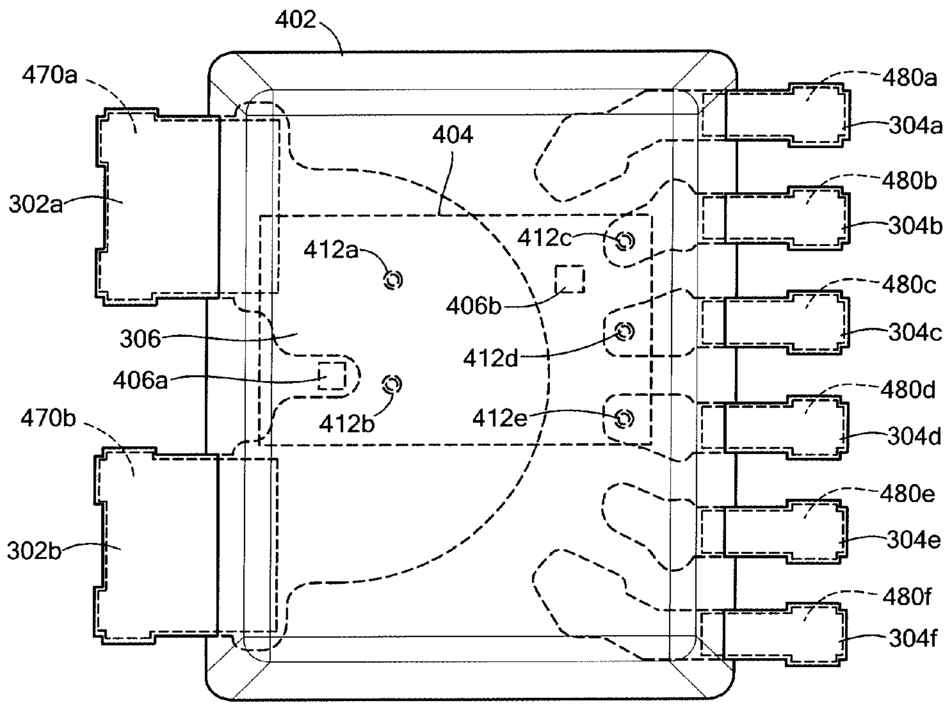
402
470a
480a
304a
404
480b
302a
304b
412c
412a
480c
406b
306
304c
412d
406a
480d
470b
412b
412e
304d
480e
302b
304e
480f
304f

FIG. 4A

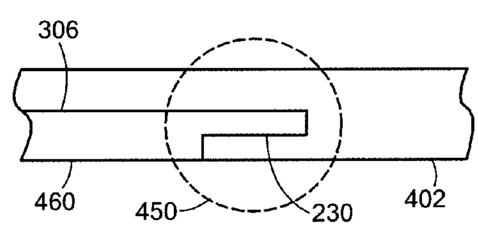
306
460
450
230
402

FIG. 4B

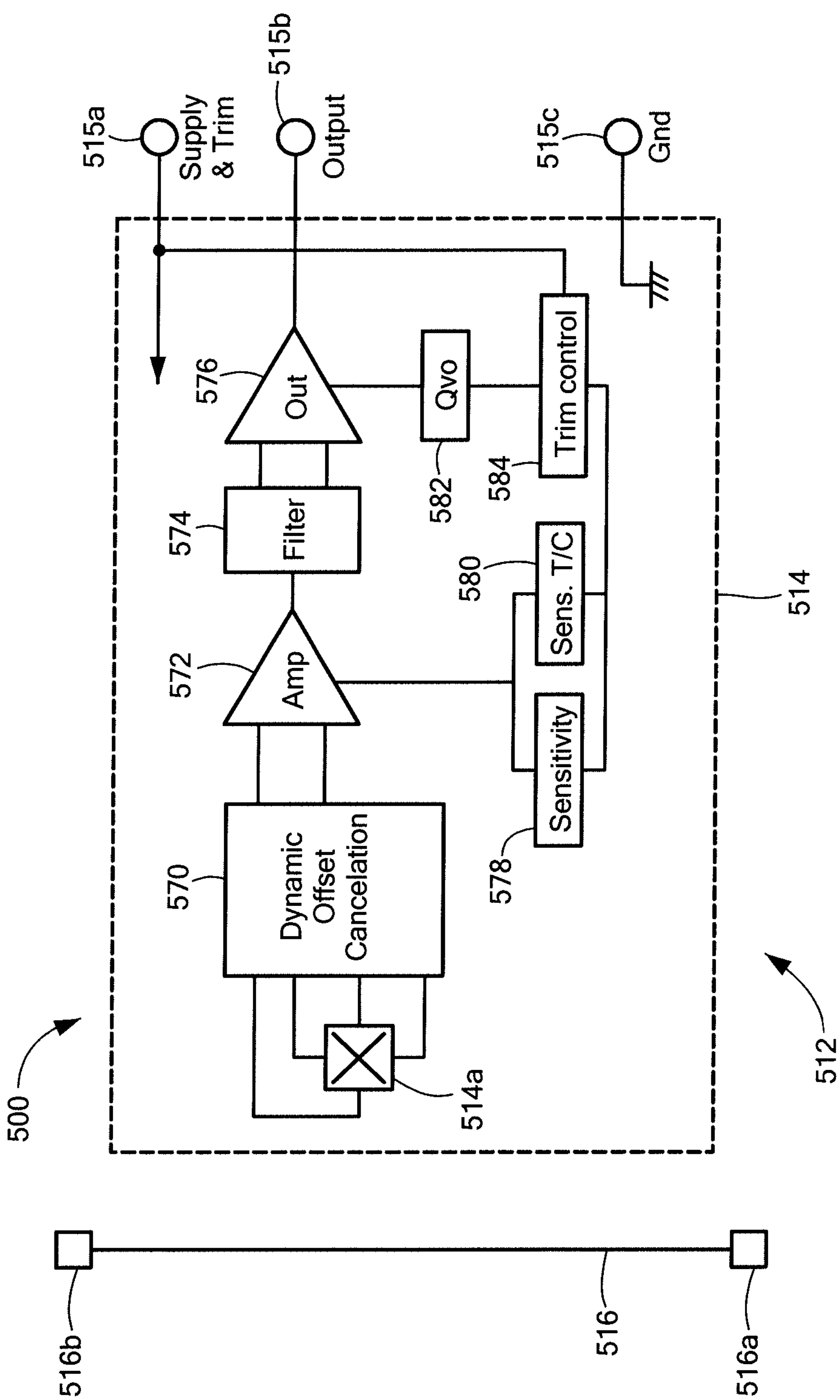
515a
Supply & Trim
515b
Output
515c
Gnd
576
Out
582
Qvo
584
Trim control
574
Filter
580
Sens. T/C
514
572
Amp
578
Sensitivity
570
Dynamic Offset Cancelation
514a
500
512
516b
516
516a

FIG. 5

PACKAGING FOR AN ELECTRONIC DEVICE

BACKGROUND

Techniques for integrated circuit (IC) packaging are well known in the art. In general, a semiconductor die is cut from a wafer, processed, and attached to a lead frame. As is known in the art, ICs are typically overmolded with a plastic or other material to form the package. After assembly of the IC package, the package may then be placed on a circuit board.

SUMMARY

In one aspect, a method includes processing a metal substrate, performing a first etch on a first surface of the metal substrate to form, for an integrated circuit package, secondary leads and a curved component having two primary leads and performing a second etch, on a second surface of the substrate opposite the first surface, at locations on the secondary leads and locations on the curved component to provide a locking mechanism. Each primary lead located at a respective end of the curved component.

In another aspect, an integrated circuit (IC) package includes a die, secondary leads, a curved component attached to the die and having two primary leads and a housing to house the die. Each primary lead is located at a respective end of the curved component. At least some of the secondary leads are attached to the die. At least one of the secondary leads includes a first recessed portion. The curved component includes a second recessed portion. At least one of the first recessed portion or the second recessed portion forms a locking mechanism.

In a further aspect, a current sensor includes a die that includes at least two magnetic field sensing elements and a curved component at least partial wrapped around one of the at least two magnetic field sensing elements and attached to the die. The curved component has a first end and a second end and is configured to receive current at one of the first end or the second end.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the invention, as well as the invention itself may be more fully understood from the following detailed description of the drawings, in which:

FIG. **1** is a flowchart of an example of a process to fabricate a package for an electronic circuit;

FIG. **2**A is a diagram of a top view of a lead frame after etching;

FIG. **2**B is a diagram of a bottom view of the lead frame after etching;

FIG. **2**C is a diagram of an angled view of the bottom of the lead frame after etching;

FIG. **3**A is a diagram of a top view of leads detached from the lead frame;

FIG. **3**B is a diagram of an angled view of the bottom of the leads detached from the lead frame;

FIG. **3**C is a diagram of an angled view of the bottom of the leads detached from the lead frame;

FIG. **4**A is a diagram of an example of an implementation of the leads in a plastic small outline flat (PSOF) lead package with a die;

FIG. **4**B is a cross-sectional view of a locking mechanism in the PSOF lead package in FIG. **4**A; and

FIG. **5** is an electronic circuit diagram of an example of a die that may be used in a PSOF lead package.

DETAILED DESCRIPTION

Described herein are techniques to fabricate a package such as a plastic small outline flat (PSOF) lead package, for example. The fabrication of the package includes fabricating leads. The leads are fabricated using a second etch process to allow easy detachability from a lead frame. The leads are also fabricated, using the second etch process, to include recessed surfaces that contribute to a locking mechanism to enable the leads to be secured with the mold compound of the package.

Referring to FIG. **1**, an example of a process to fabricate leads for use in a package for an electronic circuit is a process **100**. Process **100** applies a photoresist to surface of a metal substrate (**102**). In one example, the metal substrate is a copper substrate.

Process **100** performs photolithography on the metal substrate (**104**). In one example, a photoresist is applied to both surfaces of the metal substrate. A first mask is placed over a top surface of the metal substrate and the exposed portions of the photoresist are radiated with an ultraviolet (UV) light. A second mask is placed on a bottom surface of the metal substrate and the exposed portions of the photoresist are radiated with the UV light. The second mask exposes less portions of the photoresist and as will be described herein, these exposed portions contribute to fabricating recessed portions of the leads.

The photoresist exposed on both surfaces to the UV light is generally removed by a developer solution leaving exposed portions of the metal substrate in a pattern corresponding to the mask used for that surface. In some examples, the photoresist is baked prior to applying the first or second mask. In other examples, the photoresist is baked after the developer solution is applied. While use of positive photoresist is described herein, one of ordinary skill in the art would recognize that the photolithography process may also be performed using negative photoresist instead.

Process **100** performs a first etch on one surface of the metal substrate (**108**). For example, the exposed portions of the metal substrate are etched away. The result of the first etch is a lead frame **202** depicted in FIG. **2**A. The first etch may be performed using a dry etch or a wet etch process.

Process **100** performs a second etch on an opposite surface of the metal substrate (**114**). For example, the exposed portions of the metal substrate are etched. The second etch is performed to a depth that is less than a depth performed by the first etch leaving some portion of the metal to form the recessed portions. In one example, the second etch removes the metal down to a depth that is about 40% to 60% of a depth removed by the first etch. In one particular example, the second etch removes the metal down to a depth that is about 50% of a depth removed by the first etch. The second etch may be performed using a dry etch or a wet etch process.

The result of the second etch is a lead frame **202** depicted in FIGS. **2**B and **2**C from a bottom or angled bottom view. The portions **220** and **230** are the areas that are etched during the second etch. After the second etch, the portions **220** are used to easily detach leads from the lead frame **202**. The portions **230** are used as part of a locking mechanism to lock the leads with the mold compound as described in FIG. **4**B, for example.

It is understood by one of ordinary skill in the art that the first etch and the second etch may be performed concurrently. For example, both the top and bottom surfaces may be patterned with a respective mask and exposed to UV light prior to etching both the top surface and the bottom surface concurrently.

Process **100** removes the photoresist (**116**). For example, positive photoresist is removed using organic solvents such as acetone and negative photoresist is removed using hot sulfuric acid immersion, for example. In other examples, a photoresist stripper is used.

Process **100** attaches a die to a lead frame (**122**). For example, a die is attached to a curved component **306** and secondary leads **304***b*-**304***d* (FIGS. **3**A to **3**C) using solder bumps. In one example, the die is oriented in a flip-chip arrangement with an active surface of the die which supports electrical components adjacent to the lead frame.

Process **100** overmolds the die and a portion of the lead frame (**130**) and removes portions of the lead frame (**138**). For example, the mold compound engages the recessed portions formed by the second etch to form a locking mechanism, an example of which is shown in FIG. **4**B. In one example, the overmold material forms a housing for the package. The overmold material may be a plastic or other electrically insulative and protective material to form an integrated circuit (IC) package. Suitable materials for the non-conductive mold material include thermoset and thermoplastic mold compounds and other commercially available IC mold compounds.

Referring to FIGS. **3**A to **3**C, the process **100** is used to fabricate a lead frame **202** including primary leads **302***a*, **302***b* that are part of a curved component **306** and secondary leads **304***a*-**304***f*. In one example, the curved component **306** is in a shape of a half circle. The primary leads **302***a*, **302***b* are configured to carry current of about 100 amps. The outer two secondary leads **304***a*, **304***f* bend at an angle towards the primary leads. Each of the secondary leads includes corners such as a corner **320** on secondary lead **304***f* in FIG. **3**A. The corner **320** contributes to a more effective soldering of the secondary lead to other objects (e.g., a printed circuit board) because the solder wicks easily in the corner **320**.

FIG. **4**A is an example of the primary and secondary leads used in a PSOF lead package. For example, the PSOF lead package includes the mold compound **402**, the die **404**, the curved component **306** with primary leads **302***a*, **302***b*, and secondary leads **304***a*-**304***f*. The curved component **306** is attached to the die **404** with solder bumps **412***a*, **412***b*, for example. The secondary leads **304***b*-**304***d* are attached to the die **404** with solder bumps **412***c*, **412***d*, for example. The die **404** includes a Hall effect sensor **406***a* and a Hall effect sensor **406***b*. In one example, the curved component **306** at least partially wraps around the Hall effect sensor **406***a*.

Each area of pads attached to the primary leads **302***a*, **302***b* are generally larger than each area of pads attached to each of the secondary leads **304***a*-**304***f*. For example, pads **470***a*, **470***b* are attached to the primary leads **302***a*, **302***b*, respectively. The pads **480***a*-**480***f* are attached to the secondary leads **480***a*-**480***f*. In one example, each area of pads **470***a*, **470***b* is at least 4 times larger than each area of pads **480***a*-**480***f*. In other examples, each area of pads **470***a*, **470***b* is at least 5 to 10 times larger than each area of pads **480***a*-**480***f*.

FIG. **4**B depicts an example of a locking mechanism. For example, a curved component **306** includes the recessed portion **230** which forms a locking mechanism **450** with a mold compound **402**. While FIG. **4**A depicts a curved component **306**, the locking mechanism is also provided by the recessed portion **230** for secondary leads **304***a*-**304***f* in a manner similar to what is depicted in FIG. **4**B. The curved component **306** also forms part of a bottom portion **460** of the PSOF lead package. The primary leads **302***a*, **302***b* and the secondary leads **304***a*-**304***f* also form part of the bottom portion **460** of the PSOF lead package. The exposed leads **302***a*, **302***b*, **304***a*-**304***f* contribute to an easy soldering process.

FIG. **5** depicts a schematic representation of an example of a die that may be used in a PSOF lead package. For example, the die in FIG. **5** is a magnetic field sensor such as a current sensor **500**. The current sensor **500** includes a conductor **516** represented by a line having circuit board mounting mechanisms **516***a*, **516***b*, such as may take the form of the above-described curved component **306**. An illustrative magnetic field sensor **512** includes the sensor die **514** and leads **515**, here labeled **515***a*, **515***b*, and **515***c*. Lead **515***a* provides a power connection to the Hall effect current sensor **512**, lead **515***b* provides a connection to the current sensor output signal, and lead **515***c* provides a reference, or ground connection to the current sensor.

The magnetic field sensor includes a magnetic field sensing element **514***a* such as a Hall effect element that senses a magnetic field induced by a current flowing in the conductor **516**, producing a voltage in proportion to the magnetic field **564**. The magnetic field sensing element **514***a* is coupled to a dynamic offset cancellation circuit **570**, which provides a DC offset adjustment for DC voltage errors associated with the Hall effect element **514***a*. When the current through the conductor **516** is zero, the output of the dynamic offset cancellation circuit **570** is adjusted to be zero.

The dynamic offset cancellation circuit **570** is coupled to an amplifier **572** that amplifies the offset adjusted Hall output signal. The amplifier **572** is coupled to a filter **574** that can be a low pass filter, a high pass filter, a band pass filter, and/or a notch filter. The filter is selected in accordance with a variety of factors including, but not limited to, desired response time, the frequency spectrum of the noise associated with the magnetic field sensing element **514***a*, the dynamic offset cancellation circuit **570**, and the amplifier **572**. In one particular embodiment, the filter **574** is a low pass filter. The filter **574** is coupled to an output driver **576** that provides an enhanced power output for transmission to other electronics (not shown).

A trim control circuit **584** is coupled to lead **515***a* through which power is provided during operation. Lead **515***a* also permits various current sensor parameters to be trimmed, typically during manufacture. To this end, the trim control circuit **584** includes one or more counters enabled by an appropriate signal applied to the lead **515***a*.

The trim control circuit **584** is coupled to a quiescent output voltage (Qvo) circuit **582**. The quiescent output voltage is the voltage at output lead **515***b* when the current through conductor **516** is zero. Nominally, for a unipolar supply voltage, Qvo is equal to Vcc/2. Qvo can be trimmed by applying a suitable trim signal through the lead **515***a* to a first trim control circuit counter within the trim control circuit **584** which, in turn, controls a digital-to-analog converter (DAC) within the Qvo circuit **582**.

The trim control circuit **584** is further coupled to a sensitivity adjustment circuit **578**. The sensitivity adjustment circuit **578** permits adjustment of the gain of the amplifier **572** in order to adjust the sensitivity of the current sensor **512**. The sensitivity can be trimmed by applying a suitable trim signal through the lead **515***a* to a second trim control circuit counter within the trim control circuit **584** which, in turn, controls a DAC within the sensitivity adjustment circuit **578**.

The trim control circuit **584** is further coupled to a sensitivity temperature compensation circuit **580**. The sensitivity temperature compensation circuit **580** permits adjustment of the gain of the amplifier **572** in order to compensate for gain variations due to temperature. The sensitivity temperature compensation can be trimmed by applying a suitable trim signal through the lead **515***a* to a third trim control circuit counter within the trim control circuit **584** which, in turn, controls a DAC within the sensitivity temperature compensation circuit **580**.

It will be appreciated by those of ordinary skill in the art that the circuitry shown in FIG. **5** is illustrative only of exemplary circuitry that may be associated with and integrated into a magnetic field sensor. In another embodiment, additional circuitry may be provided for converting the magnetic field sensor into a "digital fuse" which provides a high or low output signal depending on whether the magnetic field induced by the current through the conductor **516** is greater or less than a predetermined threshold level. The additional circuitry for this alternative embodiment can include a comparator and/or a latch, and/or a relay.

In one example, a tape may be applied to the current sensor to increase the isolation voltage if desired. For example, some prior current sensors employ a layer of underfill material or have an insulating tape between die and current conductor. Examples of such devices are described in U.S. Pat. Nos. 6,356,068 and 7,075,287 (the latter being assigned to Allegro Microsystems, Inc., Assignee of the subject application).

In other examples, a die that may be used in a PSOF lead package may include at least one of a magnetic field sensing element or a magnetic field sensor.

As used herein, the term "magnetic field sensing element" is used to describe a variety of electronic elements that can sense a magnetic field. The magnetic field sensing element can be, but is not limited to, a Hall effect element, a magnetoresistance element, or a magnetotransistor. As is known, there are different types of Hall effect elements, for example, a planar Hall element, a vertical Hall element, and a Circular Vertical Hall (CVH) element. As is also known, there are different types of magnetoresistance elements, for example, a semiconductor magnetoresistance element such as Indium Antimonide (InSb), a giant magnetoresistance (GMR) element, an anisotropic magnetoresistance element (AMR), a tunneling magnetoresistance (TMR) element, and a magnetic tunnel junction (MTJ). The magnetic field sensing element may be a single element or, alternatively, may include two or more magnetic field sensing elements arranged in various configurations, e.g., a half bridge or full (Wheatstone) bridge. Depending on the device type and other application requirements, the magnetic field sensing element may be a device made of a type IV semiconductor material such as Silicon (Si) or Germanium (Ge), or a type III-V semiconductor material like Gallium-Arsenide (GaAs) or an Indium compound, e.g., Indium-Antimonide (InSb).

As used herein, the term "magnetic field sensor" is used to describe a circuit that uses a magnetic field sensing element, generally in combination with other circuits. Magnetic field sensors are used in a variety of applications, including, but not limited to, an angle sensor that senses an angle of a direction of a magnetic field, a current sensor that senses a magnetic field generated by a current carried by a current-carrying conductor, a magnetic switch that senses the proximity of a ferromagnetic object, a rotation detector that senses passing ferromagnetic articles, for example, magnetic domains of a ring magnet or a ferromagnetic target (e.g., gear teeth) where the magnetic field sensor is used in combination with a back-biased or other magnet, and a magnetic field sensor that senses a magnetic field density of a magnetic field.

The processes described herein are not limited to the specific examples described. For example, the process **100** is not limited to the specific processing order of FIG. **1**. Rather, any of the processing blocks of FIG. **1** may be re-ordered, combined or removed, performed in parallel or in serial, as necessary, to achieve the results set forth above.

Elements of different embodiments described herein may be combined to form other embodiments not specifically set forth above. Other embodiments not specifically described herein are also within the scope of the following claims.

What is claimed is:

1. An integrated circuit (IC) package comprising:

a die;

a housing to house the die;

secondary leads, at least some of the secondary leads attached to the die, at least one of the secondary leads comprising a first recessed portion at a first end of the secondary lead and a first outside portion being substantially flat and extending away from the housing, the first outside portion comprising corners at a second end of the secondary lead, opposite the first end, configured to contribute to solder wicking; and

a curved component attached to the die and having two primary leads substantially flat and extending away from the housing, each primary lead located at a respective end of the curved component, the curved component comprising a second recessed portion;

wherein at least one of the first recessed portion or the second recessed portion forms a locking mechanism with the housing,

wherein at least one surface of a secondary lead forms a bottom surface of the package, and

wherein at least one surface of the curved component forms a bottom surface of the package.

2. The IC package of claim **1**, wherein at least one of the secondary leads comprises a portion that is recessed between 40% and 60% of the total thickness of a lead.

3. The IC package of claim **2**, wherein at least one of the secondary leads comprises a portion that is recessed about 50% of the total thickness of a lead.

4. The IC package of claim **1**, wherein the curved component comprises a portion that is recessed between 40% and 60% of the total thickness of a lead.

5. The IC package of claim **4**, wherein the curved component comprises a portion that is recessed about 50% of the total thickness of a lead.

6. The IC package of claim **1**, wherein the curved component is in a shape of a semi-circle.

7. The IC package of claim **1**, wherein the die comprises at least two Hall elements.

8. The IC package of claim **7**, wherein the curved component wraps at least partially around one of the at least two Hall elements.

9. The IC package of claim **1** wherein the housing is at least 4×6 mm and the package is configured to provide current of about 100 amps to the die.

10. The IC package of claim **1** wherein each area of pads attached to a respective primary lead is at least four times larger than each area of pads attached to a respective secondary lead.

11. A current sensor disposed in a package, comprising:

a die comprising at least two magnetic field sensing elements;

a housing to house the die;

secondary leads, at least some of the secondary leads attached to the die, at least one of the secondary leads comprising a first outside portion being substantially flat and extending away from the housing, the first outside portion comprising corners configured to contribute to solder wicking; and

a curved component at least partial wrapped around one of the at least two magnetic field sensing elements and attached to the die, the curved component having a first end and a second end and configured to receive current at one of the first end or the second end, the first end and the second end being substantially flat and extending away from the housing,

wherein at least one surface of a secondary lead forms a bottom surface of the package, and

wherein at least one surface of the curved component forms a bottom surface of the package.

12. The current sensor of claim **11** wherein the at least two magnetic field sensing elements comprises at least one of a Hall effect element or a magnetoresistance element.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 9,190,606 B2
APPLICATION NO. : 13/834617
DATED : November 17, 2015
INVENTOR(S) : Shixi Louis Liu et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On The Title Page, Item (73) Assignee, delete “Micosystems” and replace with --Microsystems--.

Signed and Sealed this
Fifteenth Day of March, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office